WHAT IS CLAIMED IS:

1. An apparatus for estimating power consumption, comprising:

an behavioral synthesis unit to which an algorithm-level description is input for converting the algorithm-level description to a clock-based description and behavioral synthesis information; and

5   a clock-based simulation unit to which the clock-based description and behavioral synthesis information are input for executing a clock-based simulation and calculating a power consumption factor of a storage element based upon both the clock-based description and behavioral synthesis information.

2. The apparatus according to claim 1, wherein the power consumption factor of the storage element is calculated by discriminating the type of the storage element using the behavioral synthesis information in regard to an array-variable part.

3. The apparatus according to claim 1, wherein the power consumption factor is toggle rate and/or transition probability.

4. The apparatus according to claim 2, wherein the power consumption factor is toggle rate and/or transition probability.

5. The apparatus according to claim 1, wherein correspondence between RT variable names and gates is assumed from the behavioral synthesis information, and toggle rates and/or transition probabilities are set in gate circuits, thereafter the toggle rates and/or transition

5 probabilities of all gate circuits being calculated.

6. The apparatus according to claim 3, wherein if a gated clock is provided, the toggle rate and/or transition probability of a clock are

made the same as the write probability with respect to a storage element.

7.   A method of estimating power consumption, comprising the steps of:

inputting a clock-based description and behavioral synthesis information;

5   executing a clock-based simulation based upon the clock-based description; and

calculating a power consumption factor based upon both the clock-based description and behavioral synthesis information.

8.   The method according to claim 7, further comprising a step of calculating power consumption factor of the storage element by discriminating the type of the storage element using the behavioral synthesis information in regard to an array-variable part.

9.   The method according to claim 7, wherein the power consumption factor is toggle rate and/or transition probability.

10.   The method according to claim 8, wherein the power consumption factor is toggle rate and/or transition probability.

11.   The method according to claim 9, further comprising the steps of assuming correspondence between RT variable names and gates from the behavioral synthesis information and, setting toggle rates and/or transition probabilities in gate circuits, and, thereafter, calculating the

5   toggle rates and transition probabilities of all gate circuits.

12.   The method according to claim 9, wherein if a gated clock is provided, the toggle rate and/or transition probability of a clock are made the same as the write probability with respect to a storage element.